


[Search Results](#)
[BROWSE](#)
[SEARCH](#)
[IEEE XPLORE GUIDE](#)
[SUPPORT](#)

Results for "((test bench' <near/2> generat???) <and> 'memory models') <in> pdfdata"

Your search matched 1 of 1748191 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

[e-mail](#) [printer](#)

[Search Options](#)
[View Session History](#)
[New Search](#)
[Key](#)

IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

[Modify Search](#)

☐ Check to search only within this results set

 Display Format: ☒ Citation ☐ Citation & Abstract

[IEEE/IET](#)
[Books](#)
[Educational Courses](#)
[Application Notes](#)

Interactive online content developed from IEEE conference tutorials.

[Select All](#) [Deselect All](#)

1. Reuse of models and testbenches at different levels of abstraction

Frank, G.A.; Gray, F.G.; Gopalakrishnan, S.; Song, W.;

Verilog HDL Conference and VHDL International Users Forum, 1998. IVC/VIUF. Proceedings., 15 international

16-19 March 1998 Page(s):130 - 137

Digital Object Identifier 10.1109/IVC.1998.660691

[AbstractPlus](#) | Full Text: [PDF\(516 KB\)](#) [IEEE CNF](#)

[Rights and Permissions](#)

[Help](#) [Contact Us](#) [Privacy & Security](#)

© Copyright 2004 IEEE - All Rights Reserved

Indexed by
 Inspect